CLAIMS

We claim:

1. A circuit comprising:

an input terminal coupled to receive an analog input signal;

a plurality of sample-and-hold circuits, an input terminal of each of said plurality of sample-and-hold circuits coupled to said input terminal; and

a plurality of analog-to-digital (A/D) converters, each of said plurality of A/D converters having an input terminal and an output terminal, said input terminal being coupled to an output terminal of a corresponding one of said plurality of sample-and-hold circuits,

wherein said plurality of sample-and-hold circuits and said plurality of A/D converters are arranged in a two-dimensional array of ADC cells, each ADC cell including one of said plurality of sample-and-hold circuits coupled to one of said plurality of A/D converters, each ADC cell in said two-dimensional array of ADC cells being addressed by a row access signal and a column access signal; and

wherein said plurality of sample-and-hold circuits sample said analog input signal sequentially, storing a plurality of analog samples at each of said plurality of sample-and-hold circuits; and said plurality of A/D converters convert said plurality of analog samples in parallel to generate digital values at said output terminals representative of said analog samples.

2. The circuit of claim 1, further comprises:

a first signal generator for generating a first signal having a plurality of levels; and

a binary signal generator for generating a series of binary signals,

wherein each of said plurality of A/D converters comprises:

a comparator having a first input terminal connected to receive said first signal, said comparator having a second input terminal connected to receive said analog sample of said analog input signal to be converted into a digital value; and

a latch having a first input terminal coupled to receive an output signal of said comparator, said latch having a data input terminal coupled to receive said series of binary signals, an output signal of said comparator controlling when said latch provides an output signal corresponding to a binary signal applied to said data input terminal,

wherein said latch provides at least a portion of an N-bit digital code representing said analog sample applied to said second input terminal of said comparator.

3. The circuit of claim 1, wherein each of said plurality of sample-and-hold circuits comprises:

a switch having an input terminal coupled to receive said analog input signal and an output terminal, said switch being controlled by a select signal; and

a capacitor coupled to said output terminal of said switch.

4. The circuit of claim 1, further comprises:

an output readout circuit coupled to each of said output terminal of said plurality of A/D converters, said output readout circuit coupled to transmit sequentially said digital values from each of said plurality of A/D converters onto an output bus.

5. The circuit of claim 4, wherein said plurality of sample-and-hold circuits and said plurality of A/D converters are divided into a first bank and a second bank of sample-and-hold circuits and A/D converters, and said output readout circuit alternates between said first bank and said second bank for receiving digital values from each of said plurality of A/D converters.

6. The circuit of claim 1, wherein said digital values are provided in a bit-serial format.

7. The circuit of claim 1, wherein said digital values are provided in a parallel format.

8. The circuit of claim 1, further comprises:

a second plurality of sample-and-hold circuits, each of said second plurality of sample-and-hold circuits being coupled in parallel to a respective one of said plurality of sample-and-hold circuits,

wherein said plurality of sample-and-hold circuits and said second plurality of sample-and-hold circuits operate alternately to sample said analog input signal at different sampling times.

9. The circuit of claim 1, wherein said input terminal is a plurality of input terminals, each of said plurality of input terminals coupled to receive an analog input signal, said circuit further comprises:

a multiplexer coupled to said plurality of input terminals, said multiplexer selecting one of said plurality of input

terminals to be coupled to said plurality of sample-and-hold circuits.

10. The circuit of claim 1, wherein said plurality of sample-and-hold circuits and said plurality of A/D converters are fabricated on a single integrated circuit.

11. A circuit comprising:

an input terminal coupled to receive an analog input signal; and

a two dimensional array of ADC cells, each ADC cell including a sample-and-hold circuit coupled to an A/D converter, said array of ADC cells being addressed by a plurality of access signals,

wherein said plurality of access signals selects each sample-and-hold circuit in said array of ADC cells in sequence to cause said sample-and-hold circuits to sample said input analog signal at a plurality of sampling times and store a plurality of analog samples, and said A/D converters in said array of ADC cells convert said plurality of analog samples in parallel to generate digital values representative of said analog samples.

12. The circuit of claim 11, further comprises:

a first signal generator for generating a first signal having a plurality of levels; and

a binary signal generator for generating a series of binary signals,

wherein each of said A/D converters in said array of ADC cells comprises:

a comparator having a first input terminal connected to receive said first signal, said comparator having a second input terminal connected to receive said analog sample of said analog input signal to be converted into a digital value; and

a latch having a first input terminal coupled to receive an output signal of said comparator, said latch having a data input terminal coupled to receive said series of binary signals, an output signal of said comparator controlling when said latch provides an output signal corresponding to a binary signal applied to said data input terminal,

wherein said latch provides at least a portion of an N-bit digital code representing said analog sample applied to said second input terminal of said comparator.

13. The circuit of claim 11, wherein each of said sample-and-hold circuits in said array of ADC cells comprises:

a switch having an input terminal coupled to receive said analog input signal and an output terminal, said switch being controlled by at least one of said plurality of access signals; and

a capacitor coupled to said output terminal of said switch.

14. The circuit of claim 11, further comprises:

an output readout circuit coupled to output terminals of said A/D converters in said array of ADC cells, said output readout circuit coupled to transmit said digital values from each of said plurality of A/D converters onto an output bus.

15. The circuit of claim 14, wherein said array of ADC cells is divided into a first bank and a second bank of ADC

cells, and said output readout circuit alternates between said first bank and said second bank for receiving digital values from each of said plurality of A/D converters.

16. The circuit of claim 11, wherein said digital values are provided in a bit-serial format.

17. The circuit of claim 11, wherein said digital values are provided in a parallel format.

18. The circuit of claim 11, wherein each ADC cell further comprises a second sample-and-hold circuit coupled in parallel to said sample-and-hold circuit, said sample-and-hold circuit and said second sample-and-hold circuit in each ADC cell operate alternately to sample said analog input signal at different sampling times.

19. The circuit of claim 11, wherein said input terminal is a plurality of input terminals, each of said plurality of input terminals coupled to receive an analog input signal, said circuit further comprises:

a multiplexer coupled to said plurality of input terminals, said multiplexer selecting one of said plurality of input terminals to be coupled to said array of ADC cells.

20. The circuit of claim 19, wherein said array of ADC cells is divided into a plurality of banks of ADC cells, each bank of ADC cells being associated with one of said input terminals, and said multiplexer selects one of said plurality of input terminals to be coupled to an associated bank of ADC cells.

21. The circuit of claim 11, wherein said array of ADC cells is fabricated on a single integrated circuit.

22. A circuit comprising:

an input terminal coupled to receive an analog input signal;

a plurality of analog shift registers, an input terminal of each of said plurality of analog shift registers coupled to said input terminal; and

a plurality of analog-to-digital (A/D) converters, each of said plurality of A/D converters having an input terminal and an output terminal, said input terminal being coupled to an output terminal of a corresponding one of said plurality of analog shift registers,

wherein said plurality of analog shift registers and said plurality of A/D converters are arranged in a two-dimensional array of ADC cells, each ADC cell including one of said plurality of analog shift registers coupled to one of said plurality of A/D converters, each ADC cell in said two-dimensional array of ADC cells being addressed by a row access signal and a column access signal; and

wherein said plurality of analog shift registers sample said analog input signal sequentially, storing a plurality of analog samples at each of said plurality of analog shift registers; and said plurality of A/D converters convert said plurality of analog samples in parallel to generate digital values at said output terminal representative of said analog samples.

23. The circuit of claim 22, further comprises:

a first signal generator for generating a first signal having a plurality of levels; and

a binary signal generator for generating a series of binary signals,

wherein each of said plurality of A/D converters comprises:

a comparator having a first input terminal connected to receive said first signal, said comparator having a second input terminal connected to receive said analog sample of said analog input signal to be converted into a digital value; and

a latch having a first input terminal coupled to receive an output signal of said comparator, said latch having a data input terminal coupled to receive said series of binary signals, an output signal of said comparator controlling when said latch provides an output signal corresponding to a binary signal applied to said data input terminal,

wherein said latch provides at least a portion of an N-bit digital code representing said analog sample applied to said second input terminal of said comparator.

24. A method for performing analog-to-digital conversion comprising:

providing a two-dimensional array of ADC cells, each ADC cell including a sample-and-hold circuit coupled to an A/D converter and being addressed by a row access signal and a column access signal;

receiving an analog input signals to be converted into a digital value;

sampling said analog input signal using said two dimensional array of ADC cells, said analog input signal being sampled sequentially at a plurality of sampling times to generate a

plurality of analog samples, each analog sample being stored at a respective one of said sample-and-hold circuit in a respective ADC cell;

coupling each of said plurality of analog samples to a corresponding input terminal of a respective one of said A/D converters in said two-dimensional array of ADC cells; and

converting said plurality of analog samples to digital values at each of said A/D converters in said two-dimensional array of ADC cells.

25. The method of claim 24, wherein said converting said plurality of analog samples to digital values at each of said A/D converters in said two-dimensional array of ADC cells comprises converting said plurality of analog samples to digital values in parallel.

26. The method of claim 24, wherein said converting said plurality of analog samples to digital values at each of said A/D converters in said two-dimensional array of ADC cells comprises:

receiving a first signal having a plurality of levels;

coupling each of said plurality of analog samples to a corresponding input terminal of a comparator in a corresponding A/D converter;

at each comparator, comparing said first signal to said analog sample and outputting a comparison result;

receiving a series of binary signals at a plurality of latches; and

at each latch, applying said comparison result to a first input of said latch, and applying said series of binary signals to a data input of said latch, a logic level of said comparison

result controlling when said latch provides an output signal corresponding to a binary signal applied to said data input,

wherein said latch provides at least a portion of an N-bit digital code representing at least one of said analog samples.